REMARKS

I. Introduction

In response to the pending Office Action, Applicant has amended the specification to correct the spelling of the word buffer, which was inadvertently misspelled in a few instances. In addition, claim 1 has been amended to further clarify the intended subject matter of the present invention, as well as address the objections and rejections thereto under 35 U.S.C. § 112, second paragraph. Further, claim 3 has been amended to address the objection thereto, and claims 4 and 5 have been amended to eliminate the recitation of multiple dependent claims. New claims 6-10 track original claims 4 and 5. No new matter has been added.

For the reasons set forth below, it is respectfully submitted that all pending claims are in condition for allowance.

II. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1-5 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,108,737 to Sharma. Applicant respectfully submits that claims 1-5, as amended, are not anticipated by Sharma.

The present invention relates to a shared memory device, which includes in-part a plurality of master interface circuits, a FIFO which is coupled to the master interface circuits and a shared memory interface circuit coupled to the FIFO and operable for controlling data transfers to and from the shared memory in accordance with commands obtained from the FIFO. Fig. 1 illustrates an exemplary embodiment of the present invention, in which the master interface circuits include elements 2, 6, 10 and 14, the FIFO corresponds to element 18 and the shared

memory interface circuit corresponds to element 19.

Turning to Sharma, it is respectfully submitted that, at a minimum, Sharma does not disclose or suggest any of the foregoing features. First, it is noted that Sharma does not disclose or suggest the use of a FIFO in the embodiments shown in Figs. 1 and 2 of Sharma. Indeed, in contrast to the use of a FIFO, Sharma states that memory requests are stored in accordance with an arbitration policy, such as a "conventional round-robin algorithm" (see, col. 7, lines 55-59). Sharma also discloses the use of a "weak ordering consistency model", in which memory instructions are stored based on whether or not a given instruction requires ordering relative to the other instructions (see, col. 8, lines 16-29). Sharma does not appear to disclose or suggest the use of a FIFO in the embodiments illustrated in Figs. 1 and 2.

In the pending rejection it is asserted that elements 522-536 correspond to the FIFO and that these elements are provided between the master interfaces 202-208 and the shared memory 150. This conclusion is clearly in error. Fig. 5 illustrates a schematic diagram of the hierarchical switch 500 illustrated in Fig. 4 of Sharma, which relates to wholly separate embodiment. There does not appear to be any disclosure or suggestion that the hierarchical switch 500 of Sharma can be utilized in the embodiments shown in Figs. 1 and 2. As such, it is clear that Sharma does not disclose the use of a FIFO as recited by the pending claims.

Continuing, it is also clear that Sharma fails to disclose the recited master interface circuits or the shared memory interface circuit. As recited by claim 1, each master interface circuit is coupled between a given one of the masters and read/write buffers, and each master interface circuit is also coupled to the FIFO. Referring to Fig. 1 of Sharma and the pending rejection, the asserted masters 102-108 are directly connected to the asserted read and write

buffers 212-218, 222-228. As such, it is clear that Sharma does not disclose the recited master interface circuits.

Further, it is also clear that Sharma does not disclose or suggest the recited the shared memory interface circuit. As recited by the pending claims, the shared memory interface circuit is coupled to the FIFO. As Sharma does not disclose the use of a FIFO, Sharma does not disclose a shared memory interface circuit coupled to the FIFO.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and Sharma fails to do so for at least the foregoing reasons, it is clear that Sharma does not anticipate amended claim 1, or any claim dependent thereon.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that

all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

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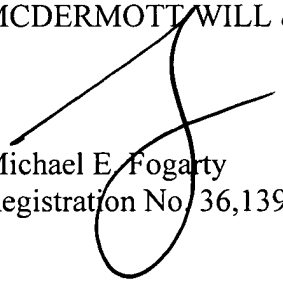

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